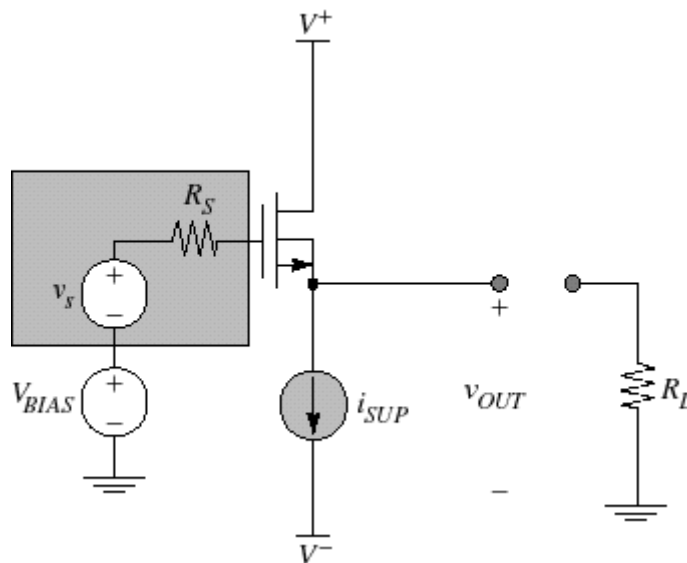


Common-Drain Amplifier

- * Also called a “source follower” for reasons that will become clear shortly



For DC bias, neglect small signal source (and its resistance) and the small-signal load resistance; $i_{SUP} = I_{SUP}$

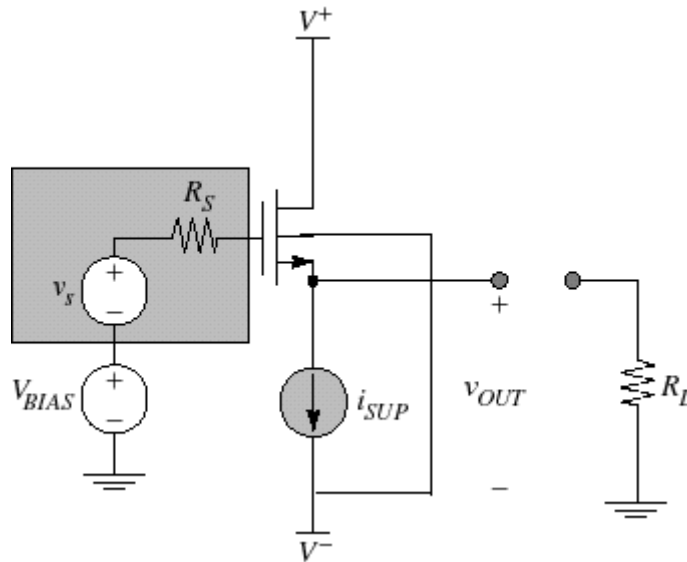
Note that

$$V_{OUT} = V_{BIAS} - V_{GS}$$

The DC gate-source voltage is:

DC Transfer Curve

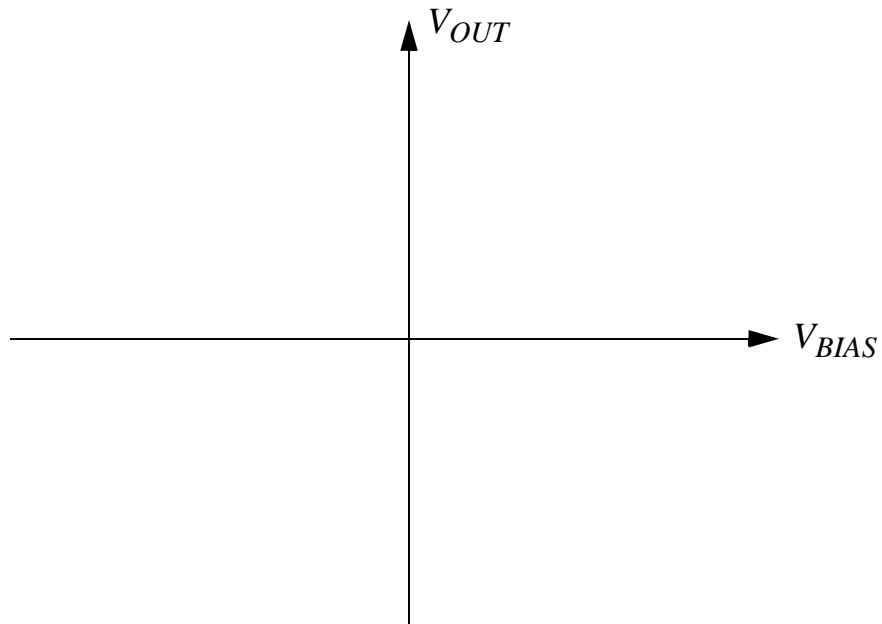
p-well CMOS process means that the source and bulk can be shorted ... not true for an n-well process.



The threshold voltage V_{Tn} is not a constant, since the source-bulk voltage V_{SB} increases as V_{OUT} increases:

$$V_{Tn} = V_{TOn} + \gamma_n \left[\sqrt{(V_{OUT} - V^-) - 2\phi_p} - \sqrt{2\phi_p} \right]$$

DC Transfer Curve for Common-Drain Amps



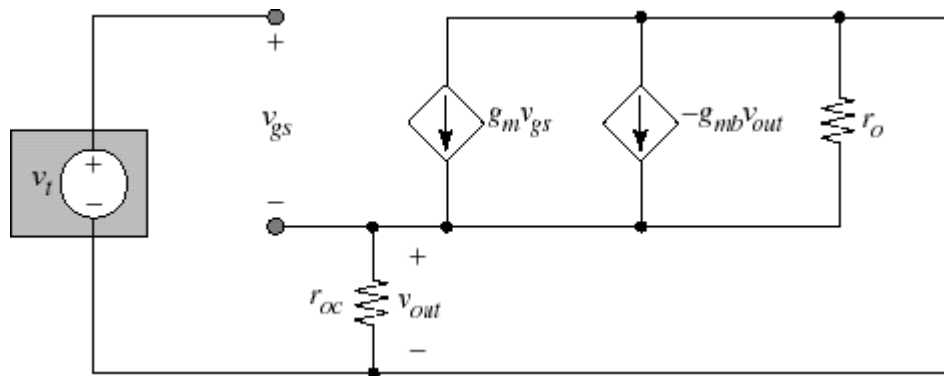
Simple idea: slope of transfer curve is the voltage gain ... about 1

The common-drain is a *voltage buffer*

$$A_v = \frac{dv_{OUT}}{dv_{BIAS}} \approx 1$$

Common-Drain Open-Circuit Voltage Gain

For finding A_v exactly, remove the source and its resistance and the load resistance ... apply a test voltage and find the output voltage



KCL at source node:

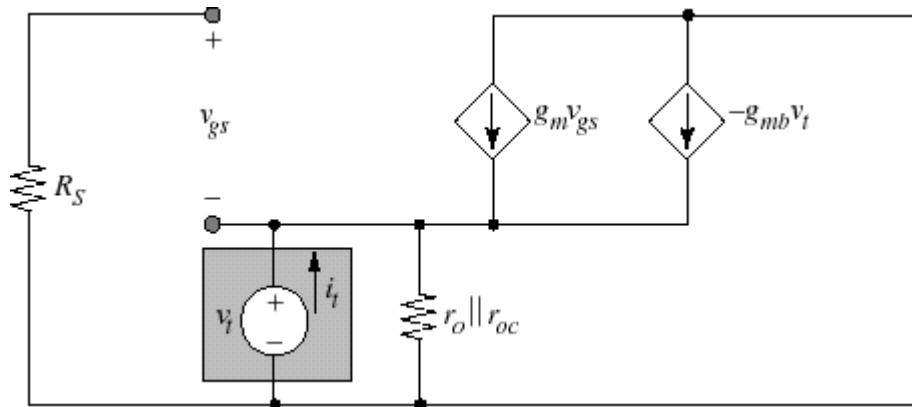
$$\frac{v_{out}}{r_{oc} || r_o} - g_m(v_t - v_{out}) - (-g_{mb}v_{out}) = 0$$

$$v_{out} \left(\frac{1}{r_{oc} || r_o} + g_m + g_{mb} \right) = g_m v_t$$

$$A_v = \frac{v_{out}}{v_t} = \frac{g_m}{g_m + g_{mb} + \left(\frac{1}{r_{oc} || r_o} \right)} \approx \frac{g_m}{g_m + g_{mb}}$$

Output Resistance of Common-Drain Amplifier

- * Leave the source resistance attached while exercising the output with a test voltage



KCL at the source node ... remove $r_o \parallel r_{oc}$ and put it back in

$$i_t + g_m(0 - v_t) + (-g_{mb}v_t) = 0$$

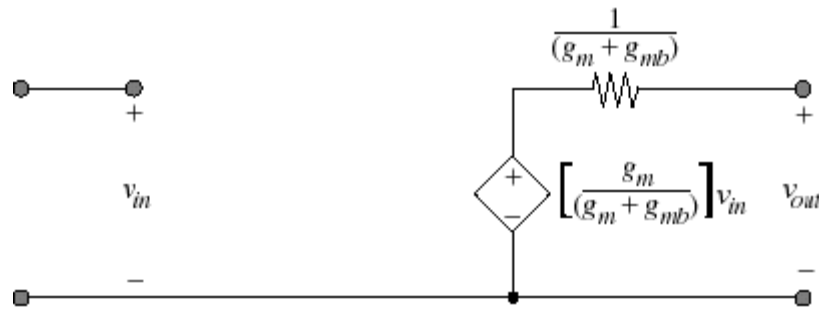
$$R_{out} = (r_o \parallel r_{oc}) \parallel \left(\frac{v_t}{i_t} \right) = (r_o \parallel r_{oc}) \parallel \left(\frac{1}{g_m + g_{mb}} \right) = \frac{1}{[1/(r_o \parallel r_{oc})] + g_m + g_{mb}}$$

Typically, $r_o \parallel r_{oc} \gg g_m + g_{mb}$

$$R_{out} \cong \frac{1}{g_m + g_{mb}}$$

Common-Drain Small-Signal Model

Input resistance is infinite: open-circuit from gate-source



If source and bulk can be shorted (possible for a MOSFET in a well), then the gate is essentially 1 (since backgate generator has zero v_{sb} controlling it.)

Output resistance is ideally zero for a voltage-output amplifier: typical values

$$g_m = 500 \mu\text{S}$$

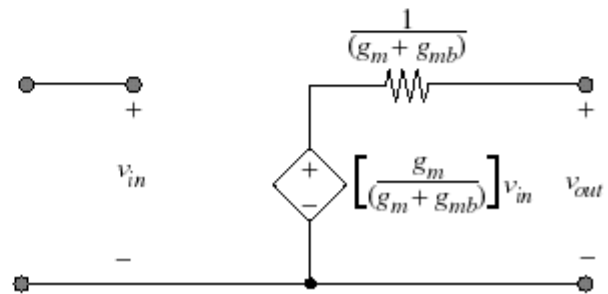
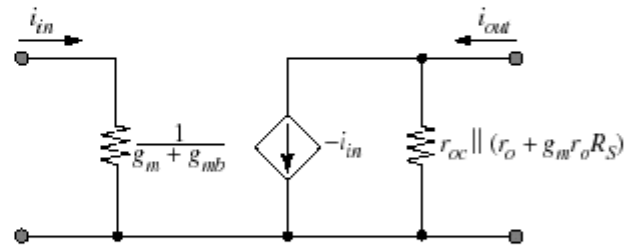
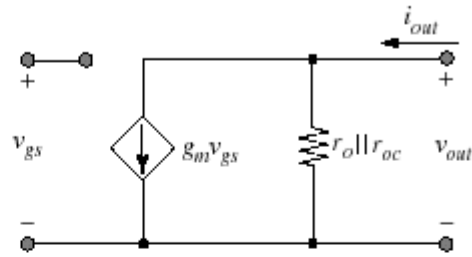
$$g_{mb} = 50 \mu\text{S}$$

$$R_{out} = \frac{1}{g_m + g_{mb}} \approx 2 \text{ k}\Omega$$

The output resistance can be reduced by increasing the transconductance ...
(W/L) can be made huge in order to drive R_{out} toward zero.

Summary of MOSFET Two-Port Models

	Transistor Type	
	NMOS	PMOS
Common Source/ Common Emitter (CS/CE)		
Common Gate/ Common Base (CG/CB)		
Common Drain/ Common Collector (CD/CC)		



Assessment of MOS Amplifiers

Common-source is the only stage that provides gain

Common-gate can buffer a poor current source into a nearly ideal one

Common-drain can buffer a poor voltage source into a nearly ideal one

We need more than one stage to approach an ideal amplifier (of any of the 4 types)