

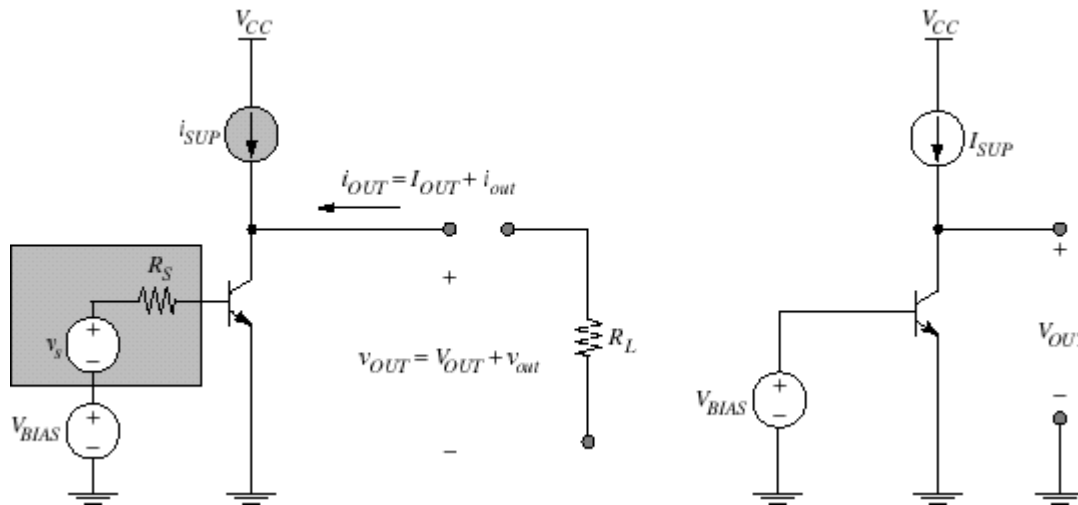
# nnp BJT Amplifier Stages: Common-Emitter (CE)

## 1. Bias amplifier in high-gain region

Note that the source resistor  $R_S$  and the load resistor  $R_L$  are *removed* for determining the bias point; the small-signal source is ignored, as well.

Use the load-line technique to find  $V_{BIAS} = V_{BE}$  and  $I_C = I_{SUP}$ .

## 2. Determine two-port model parameters



## Small-Signal Model of CE Amplifier

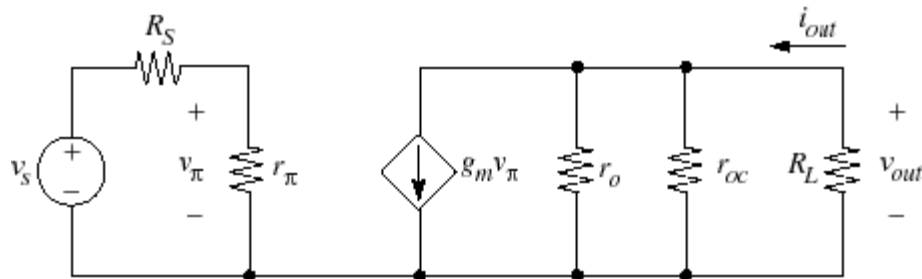
- \* The small-signal model is evaluated at the bias point; we assume that the current gain is  $\beta_o = 100$  and the Early voltage is  $V_{An} = 25$  V:

$$g_m = I_C / V_{th} \text{ (at room temperature)}$$

$$r_\pi = \beta_o / g_m = 10 \text{ k}\Omega$$

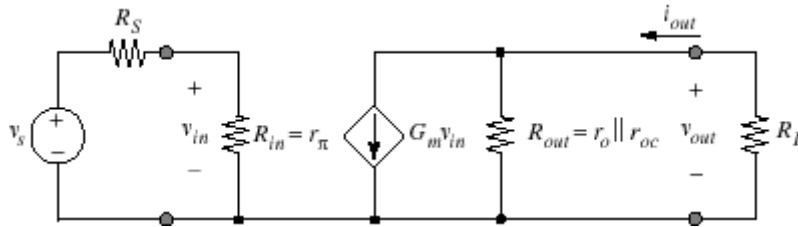
$$r_o = V_{An} / I_C = 100 \text{ k}\Omega$$

- \* Substitute small-signal model for BJT;  $V_{CC}$  and  $V_{BIAS}$  are short-circuited for small-signals



## Two-Port Model: CE Amplifier

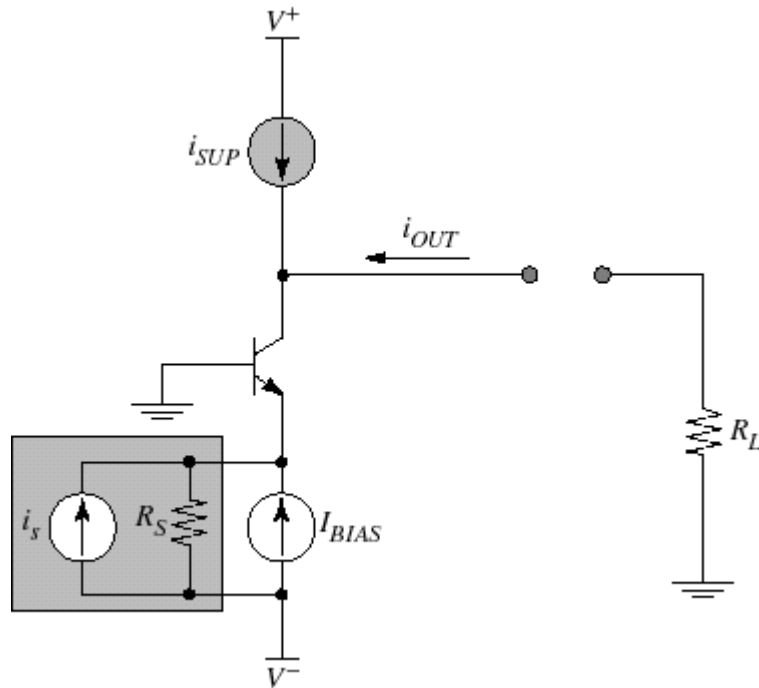
- \* Use transconductance amplifier form for model (*not* mandatory)
- \*  $R_{in} = r_{\pi}$ ,  $R_{out} = r_o \parallel r_{oc}$ ,  $G_m = g_m$  by inspection



- \* Compare with CS amplifier  
inferior input resistance  
superior transconductance  
about the same output resistance (assuming  $r_o$  dominates)

# Common-Base Amplifier

Input current is applied to the emitter (with a bias current source) and the output current is taken from the collector

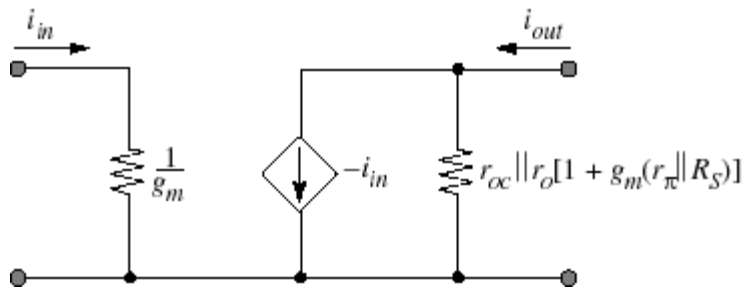


## Common Base Two-Port Model

\* See text for details of nodal analysis

$$R_{in} \cong 1/g_m, R_{out} \cong r_{oc} \parallel [r_o(1 + g_m(r_\pi \parallel R_S))], A_i = -\beta_o/(1 + \beta_o) \cong -1$$

\* CB stage is an excellent current buffer



Comparison with the CG stage:

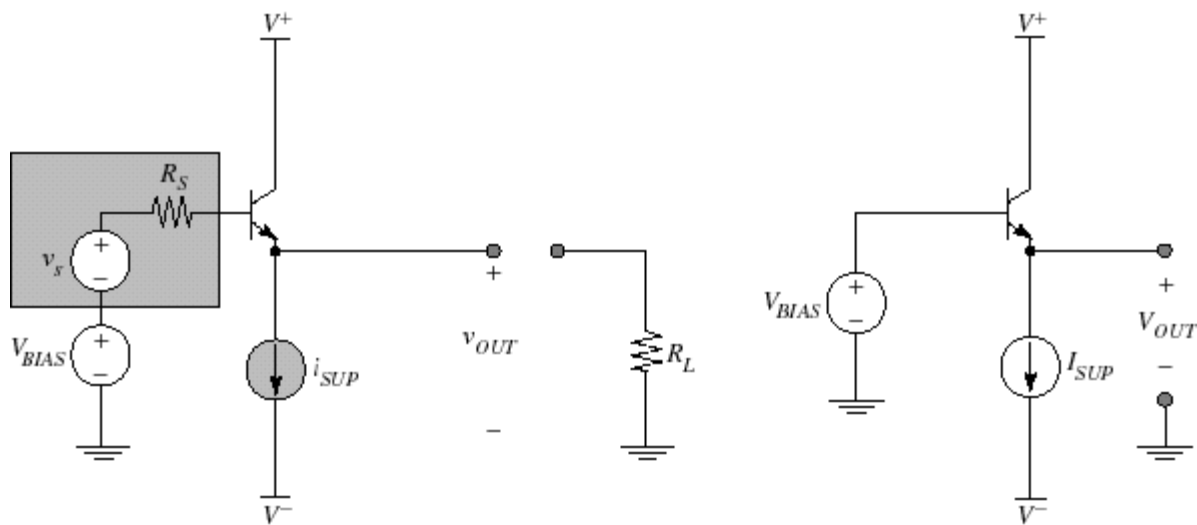
note the effect of the source resistance on the output resistance

if  $R_S$  is much greater than  $r_\pi$ , then the output resistance is approximately:

$$R_{out} \approx r_{oc} \parallel [\beta r_o]$$

# Common-Collector Amplifier

- \* Circuit configuration



- \* Biasing: if transistor is “on” (i.e., not cutoff), then

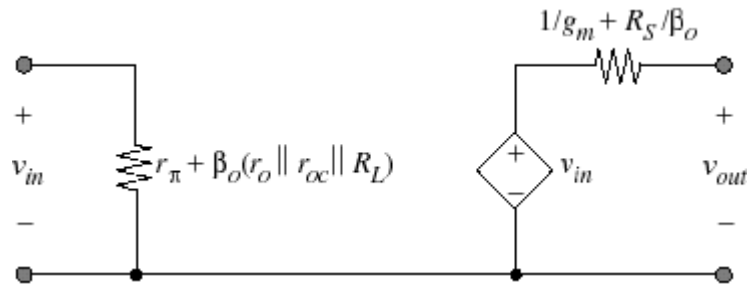
$$V_{BIAS} - V_{OUT} = 0.7 \text{ V. Plot --}$$

Alternative name ... emitter follower

## Common Collector Two-Port Model

\* Two-port model:

presence of  $r_p$  makes the analysis more involved than for a common drain



Note 1: both the input and the output resistances depend on the load and source resistances, respectively (note typo in Fig. 8.47 in text)

Note 2: this model is approximate and can give erroneous results for extremely low values of  $R_L$ . However, it is very convenient for hand analysis.

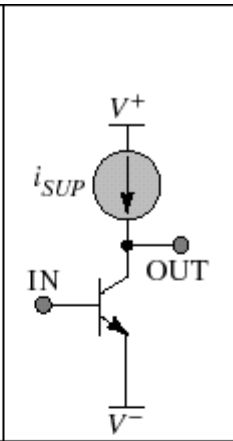
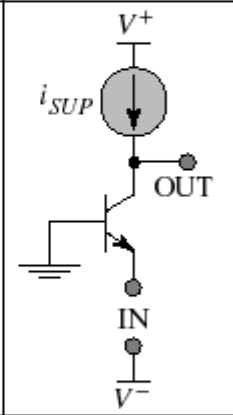
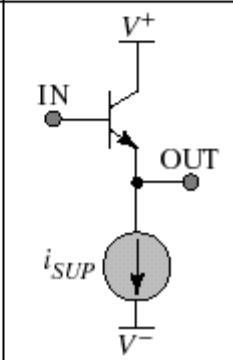
Comparison with CD stage:

CC's input resistance: high but not infinity

CC's output resistance: generally lower (but watch out for large  $R_S$ )

# Summary of BJT Single-Stage Amplifiers

Why no pnp's?

Common Emitter (CE)	
Common Base (CB)	
Common Collector (CC)	

# Single-Stage MOS and BJT Amplifier

Amplifier Type	Transistor Type		
	NMOS	PMOS	nnp
Common Source/ Common Emitter (CS/CE)			
Common Gate/ Common Base (CG/CB)			
Common Drain/ Common Collector (CD/CC)			